8M-BIT [1Mx8/512Kx16] CMOS FLASH MEMORY

FEATURES

- 1,048,576 x 8/524,288 x 16 switchable
- Single power supply operation
  - 5.0V only operation for read, erase and program operation
- Fast access time: 70/90/120ns
- Low power consumption
  - 50mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - Byte/word Programming (7us/12us typical)
  - Sector Erase (Sector structure 16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x15)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends sector erase operation to read data from, or program data to, another sector that is not being erased, then resumes the erase.
- Status Reply
  - Data polling & Toggle bit for detection of program and erase operation completion.
- Ready/Busy pin (RY/BY)
  - Provides a hardware method of detecting program or erase operation completion.
- Sector protection
  - Sector protect/chip unprotect for 5V/12V system.
  - Hardware method to disable any combination of sectors from program or erase operations
  - Temporary sector unprotect allows code changes in previously locked sectors.
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Code Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash

GENERAL DESCRIPTION

The MX29F800T/B is a 8-mega bit Flash memory organized as 1M bytes of 8 bits or 512K words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F800T/B is packaged in 44-pin SOP, 48-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29F800T/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F800T/B has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F800T/B uses a command register to manage this functionality. The command register allows for 100%
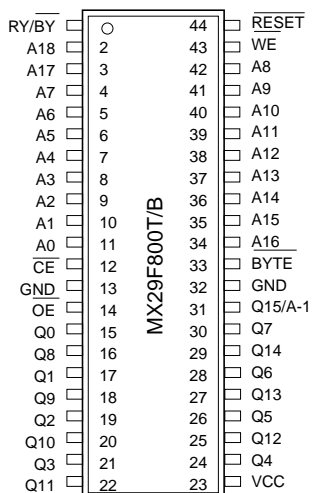
TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29F800T/B uses a 5.0V±10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

MX29F800T/B

PIN CONFIGURATIONS

44 SOP(500 mil)

```
RY/BY ⊏  ○  1      44 ⊐ RESET
 A18  ⊏     2      43 ⊐ WE
 A17  ⊏     3      42 ⊐ A8
  A7  ⊏     4      41 ⊐ A9
  A6  ⊏     5      40 ⊐ A10
  A5  ⊏     6      39 ⊐ A11
  A4  ⊏     7      38 ⊐ A12
  A3  ⊏     8      37 ⊐ A13
  A2  ⊏     9      36 ⊐ A14
  A1  ⊏    10      35 ⊐ A15
  A0  ⊏    11      34 ⊐ A16
  CE  ⊏    12      33 ⊐ BYTE
 GND  ⊏    13      32 ⊐ GND
  OE  ⊏    14      31 ⊐ Q15/A-1
  Q0  ⊏    15      30 ⊐ Q7
  Q8  ⊏    16      29 ⊐ Q14
  Q1  ⊏    17      28 ⊐ Q6
  Q9  ⊏    18      27 ⊐ Q13
  Q2  ⊏    19      26 ⊐ Q5
 Q10  ⊏    20      25 ⊐ Q12
  Q3  ⊏    21      24 ⊐ Q4
 Q11  ⊏    22      23 ⊐ VCC
```
MX29F800T/B

48 TSOP (Standard Type) (12mm x 20mm)

```
 A15  ⊏  1  ○           48 ⊐ A16
 A14  ⊏  2              47 ⊐ BYTE
 A13  ⊏  3              46 ⊐ GND
 A12  ⊏  4              45 ⊐ Q15/A-1
 A11  ⊏  5              44 ⊐ Q7
 A10  ⊏  6              43 ⊐ Q14
  A9  ⊏  7              42 ⊐ Q6
  A8  ⊏  8              41 ⊐ Q13
  NC  ⊏  9              40 ⊐ Q5
  NC  ⊏ 10              39 ⊐ Q12
  WE  ⊏ 11              38 ⊐ Q4
RESET ⊏ 12  MX29F800T/B 37 ⊐ VCC
  NC  ⊏ 13              36 ⊐ Q11
  NC  ⊏ 14              35 ⊐ Q3
RY/BY ⊏ 15              34 ⊐ Q10
 A18  ⊏ 16              33 ⊐ Q2
 A17  ⊏ 17              32 ⊐ Q9
  A7  ⊏ 18              31 ⊐ Q1
  A6  ⊏ 19              30 ⊐ Q8
  A5  ⊏ 20              29 ⊐ Q0
  A4  ⊏ 21              28 ⊐ OE
  A3  ⊏ 22              27 ⊐ GND
  A2  ⊏ 23              26 ⊐ CE
  A1  ⊏ 24              25 ⊐ A0
```

PIN DESCRIPTION

| SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE	Chip Enable Input
WE	Write Enable Input
BYTE	Word/Byte Selection input
RESET	Hardware Reset Pin/Sector Protect Unlock
OE	Output Enable Input
RY/BY	Ready/Busy Output
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK STRUCTURE

MX29F800T TOP BOOT SECTOR ADDRESS TABLE

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/Kwords)	Address Range (in hexadecimal)	
									(x16) Address Range	(x8) Address Range
SA0	0	0	0	0	X	X	X	64/32	00000h-07FFFh	00000h-0FFFFh
SA1	0	0	0	1	X	X	X	64/32	08000h-0FFFFh	10000h-1FFFFh
SA2	0	0	1	0	X	X	X	64/32	10000h-17FFFh	20000h-2FFFFh
SA3	0	0	1	1	X	X	X	64/32	18000h-1FFFFh	30000h-3FFFFh
SA4	0	1	0	0	X	X	X	64/32	20000h-27FFFh	40000h-4FFFFh
SA5	0	1	0	1	X	X	X	64/32	28000h-2FFFFh	50000h-5FFFFh
SA6	0	1	1	0	X	X	X	64/32	30000h-37FFFh	60000h-6FFFFh
SA7	0	1	1	1	X	X	X	64/32	38000h-3FFFFh	70000h-7FFFFh
SA8	1	0	0	0	X	X	X	64/32	40000h-47FFFh	80000h-8FFFFh
SA9	1	0	0	1	X	X	X	64/32	48000h-4FFFFh	90000h-9FFFFh
SA10	1	0	1	0	X	X	X	64/32	50000h-57FFFh	A0000h-AFFFFh
SA11	1	0	1	1	X	X	X	64/32	58000h-5FFFFh	B0000h-BFFFFh
SA12	1	1	0	0	X	X	X	64/32	60000h-67FFFh	C0000h-CFFFFh
SA13	1	1	0	1	X	X	X	64/32	68000h-6FFFFh	D0000h-DFFFFh
SA14	1	1	1	0	X	X	X	64/32	70000h-77FFFh	E0000h-EFFFFh
SA15	1	1	1	1	0	X	X	32/16	78000h-7BFFFh	F0000h-F7FFFh
SA16	1	1	1	1	1	0	0	8/4	7C000h-7CFFFh	F8000h-F9FFFh
SA17	1	1	1	1	1	0	1	8/4	7D000h-7DFFFh	FA000h-FBFFFh
SA18	1	1	1	1	1	1	X	16/8	7E000h-7FFFFh	FC000h-FFFFFh

MX29F800B BOTTOM BOOT SECTOR ADDRESS TABLE

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/Kwords)	Address Range (in hexadecimal)	
									(x16) Address Range	(x8) Address Range
SA0	0	0	0	0	0	0	X	16/8	00000h-01FFFh	00000h-03FFFh
SA1	0	0	0	0	0	1	0	8/4	02000h-02FFFh	04000h-05FFFh
SA2	0	0	0	0	0	1	1	8/4	03000h-03FFFh	06000h-07FFFh
SA3	0	0	0	0	1	X	X	32/16	04000h-07FFFh	08000h-0FFFFh
SA4	0	0	0	1	X	X	X	64/32	08000h-0FFFFh	10000h-1FFFFh
SA5	0	0	1	0	X	X	X	64/32	10000h-17FFFh	20000h-2FFFFh
SA6	0	0	1	1	X	X	X	64/32	18000h-1FFFFh	30000h-3FFFFh
SA7	0	1	0	0	X	X	X	64/32	20000h-27FFFh	40000h-4FFFFh
SA8	0	1	0	1	X	X	X	64/32	28000h-2FFFFh	50000h-5FFFFh
SA9	0	1	1	0	X	X	X	64/32	30000h-37FFFh	60000h-6FFFFh
SA10	0	1	1	1	X	X	X	64/32	38000h-3FFFFh	70000h-7FFFFh
SA11	1	0	0	0	X	X	X	64/32	40000h-47FFFh	80000h-8FFFFh
SA12	1	0	0	1	X	X	X	64/32	48000h-4FFFFh	90000h-9FFFFh
SA13	1	0	1	0	X	X	X	64/32	50000h-57FFFh	A0000h-AFFFFh
SA14	1	0	1	1	X	X	X	64/32	58000h-5FFFFh	B0000h-BFFFFh
SA15	1	1	0	0	X	X	X	64/32	60000h-67FFFh	C0000h-CFFFFh
SA16	1	1	0	1	X	X	X	64/32	68000h-6FFFFh	D0000h-DFFFFh
SA17	1	1	1	0	X	X	X	64/32	70000h-77FFFh	E0000h-EFFFFh
SA18	1	1	1	1	X	X	X	64/32	78000h-7FFFFh	F0000h-FFFFFh

Note: Address range is A18:A-1 in byte mode and A18:A0 in word mode.

BLOCK DIAGRAM
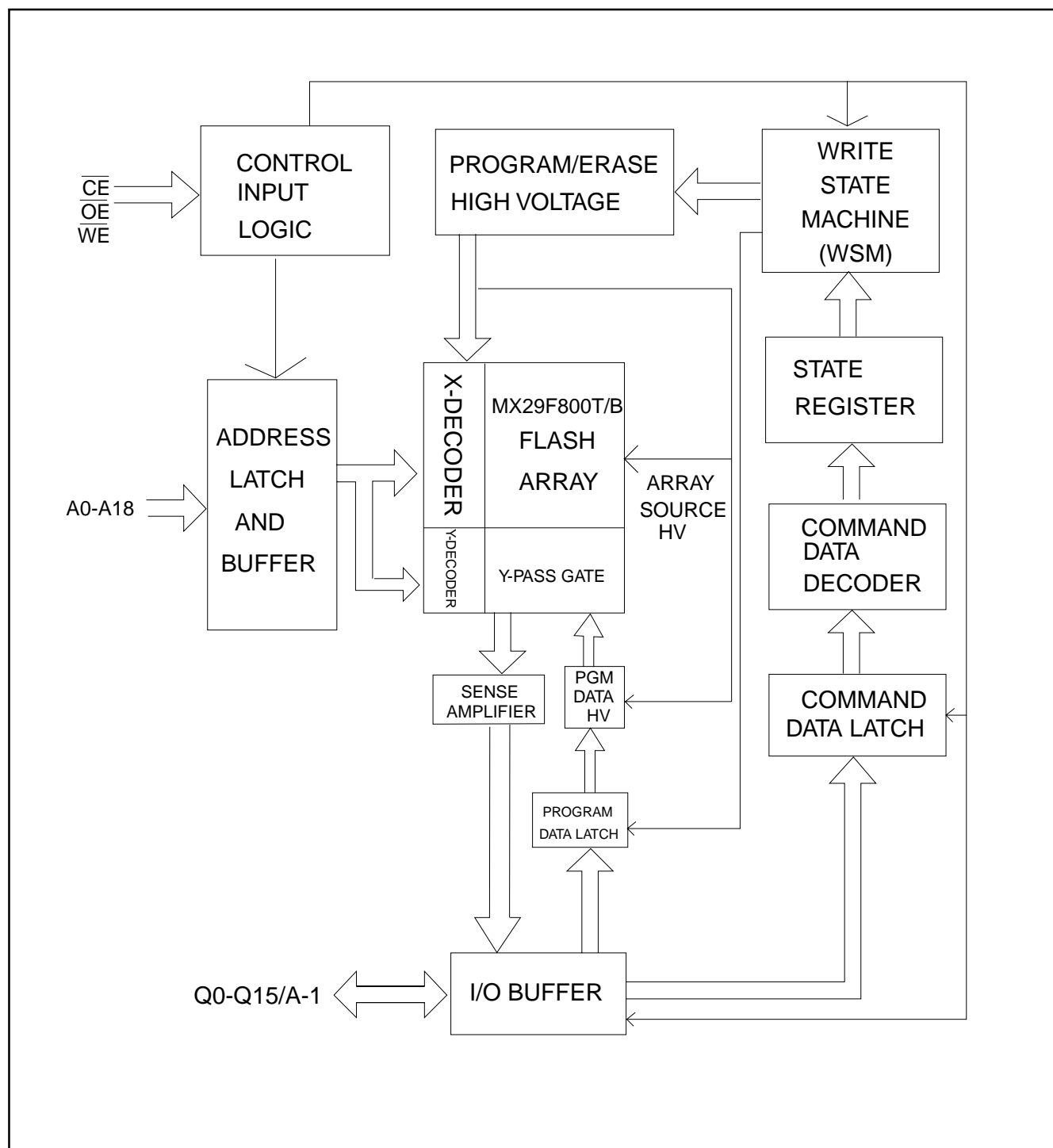
AUTOMATIC PROGRAMMING

The MX29F800T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29F800T/B is less than 8 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 8 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29F800T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F800T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE 1. SOFTWARE COMMAND DEFINITIONS

Command		Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset		1	XXXH	F0H										
Read		1	RA	RD										
Read Silicon ID	Word	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	ADI	DDI				
Sector Protect Verify	Word	4	555H	AAH	2AAH	55H	555H	90H	(SA) x02H	XX00H XX01H				
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	(SA) x04H	00H 01H				
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
	Byte	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD				
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SA	30H
Sector Erase Suspend		1	XXXH	B0H										
Sector Erase Resume		1	XXXH	30H										

Note:
1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacture code, A1=0, A0 = 1 for device code. A2-A18=do not care. (Refer to table 3)
   DDI = Data of Device identifier : C2H for manufacture code, D6H/58H (x8) and 22D6H/2258H (x16) for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address to the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 in word mode/AAAH or 555H to Address A10~A-1 in byte mode.
   Address bit A11~A18=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A18 in either state.
4. For Sector Protect Verify operation: If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

TABLE 2. MX29F800T/B BUS OPERATION

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	Q0 ~ Q15
Read Silicon ID Manufacturer Code(1)	L	L	H	L	L	X	V_{ID}(2)	C2H (Byte mode) 00C2H (Word mode)
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V_{ID}(2)	D6H/58H (Byte mode) 22D6H/2258H (Word mode)
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(3)
Sector Protect(6)	L	V_{ID}(2)	L	X	X	L	V_{ID}(2)	X
Chip Unprotect	L	V_{ID}(2)	L	X	X	H	V_{ID}(2)	X
Verify Sector Protect(6)	L	L	H	X	H	X	V_{ID}(2)	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H/0000H means unprotected.
   Code=01H/0001H means protected.
6. A18~A12=Sector address for sector protect.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage (VID). However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F800T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H/00C2H. A read cycle with A1=VIL, A0=VIH returns the device code of D6H/22D6H for MX29F800T, 58H/2258H for MX29F800B.

SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$, whichever happens first pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. EXPANDED SILICON ID CODE

Pins		A0	A1	Q15~Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	Word	VIL	VIL	00H	1	1	0	0	0	0	1	0	00C2H
	Byte	VIL	VIL	X	1	1	0	0	0	0	1	0	C2H
Device code	Word	VIH	VIL	22H	1	1	0	1	0	1	1	0	22D6H
for MX29F800T	Byte	VIH	VIL	X	1	1	0	1	0	1	1	0	D6H
Device code	Word	VIH	VIL	22H	0	1	0	1	1	0	0	0	2258H
for MX29F800B	Byte	VIH	VIL	X	0	1	0	1	1	0	0	0	58H
Sector Protection		X	VIH	X	0	0	0	0	0	0	0	1	01H (Protected)
Verification		X	VIH	X	0	0	0	0	0	0	0	0	00H (Unprotected)

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array

(no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later, while the command (data) is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. Each successive sector load cycle started by the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later must begin within 30us from the rising edge of the preceding $\overline{WE}$ or $\overline{CE}$, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (B0H) during the time-out period resets the device to read mode.

TABLE 4. WRITE OPERATION STATUS

	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2	$\overline{RY/\overline{BY}}$
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A	0

Note:
1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits.
   See "Q5:Exceeded Timing Limits " for more information.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 100us to suspend the erase operations. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the $\overline{WE}$ or $\overline{CE}$, whichever happens first. The rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first, also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode (no program verify command is required).

DATA POLLING-Q7

The MX29F800T/B also features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ $\overline{Polling}$ feature is valid after the rising edge of the fourth $\overline{WE}$ or $\overline{CE}$, whichever happens first pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The Data $\overline{Polling}$ $\overline{feature}$ is valid after the rising edge of the sixth $\overline{WE}$ or $\overline{CE}$, whichever happens first pulse of six write pulse sequences for automatic chip/ sector erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out. (see section Q3 Sector Erase Timer)

RY/$\overline{BY}$:Ready/$\overline{Busy}$

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Automatic Erase/Program algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to Vcc.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.)If the output is high (Ready), the

device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

TABLE 4 shows the outputs for RY/BY.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first, in the command sequence(prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2 us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 4 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first, in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be re-used, (other sectors are still functional and can be re-used).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DATA PROTECTION

The MX29F800T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

TEMPORARY SECTOR UNPROTECT

This feature allows temporary unprotection of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as un-protected sector. Once VID is remove from the $\overline{RESET}$ pin, all the previously protected sectors are protected again.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

SECTOR PROTECTION

The MX29F800T/B features hardware sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{OE}$, (suggest VID = 12V) A6 = VIL and $\overline{CE}$ = VIL. (see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{CE}$ and $\overline{OE}$ at VIL and $\overline{WE}$ at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT

The MX29F800T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

POWER-UP SEQUENCE

The MX29F800T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 125°C (*)
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9 & $\overline{OE}$	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.
* The automotive grade is under development.

CAPACITANCE   TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

DC CHARACTERISTICS   TA = 0°C TO 70°C, -40°C TO 125°C(Note 3), VCC = 5V±10%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			± 1	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE}$ = VIH
ISB2			0.2(Note3)	5(Note3)	uA	$\overline{CE}$ = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=1MHz
ICC2				50	mA	IOUT= 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(Note 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH1	Output High Voltage (TTL)	2.4			V	IOH = -2mA
VOH2	Output High Voltage (CMOS)	VCC-0.4			V	IOH = -100uA, VCC=VCC MIN

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. ISB2 20uA max. for automotive grade. Which is under development.

AC CHARACTERISTICS   TA = 0°C TO 70°C, -40°C TO 125°C(Note 2), VCC = 5V±10%

SYMBOL	PARAMETER	29F800T/B-70		29F800T/B-90		29F800T/B-12		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		70		90		120	ns	$\overline{CE}=\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		70		90		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		40		40		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	30	0	30	0	30	ns	$\overline{CE}$=VIL
tOH	Address to Output hold							ns	$\overline{CE}=\overline{OE}$=VIL

TEST CONDITIONS:
- Input pulse levels: 0.45V/2.4V
- Input rise and fall times is equal to or less than 10ns
- Output load: 1 TTL gate + 100pF (Including scope and jig) for MX29F800T/B-90 & MX29F800T/B-12. 1 TTL gate + 30pF (Including scope and jig) for MX29F800T/B-70.
- Reference levels for measuring timing: 0.8V, 2.0V

NOTE:
1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Automotive grade is only provided for MX29F800T/B-90 & MX29F800T/B-12. Which are under development.

READ TIMING WAVEFORMS
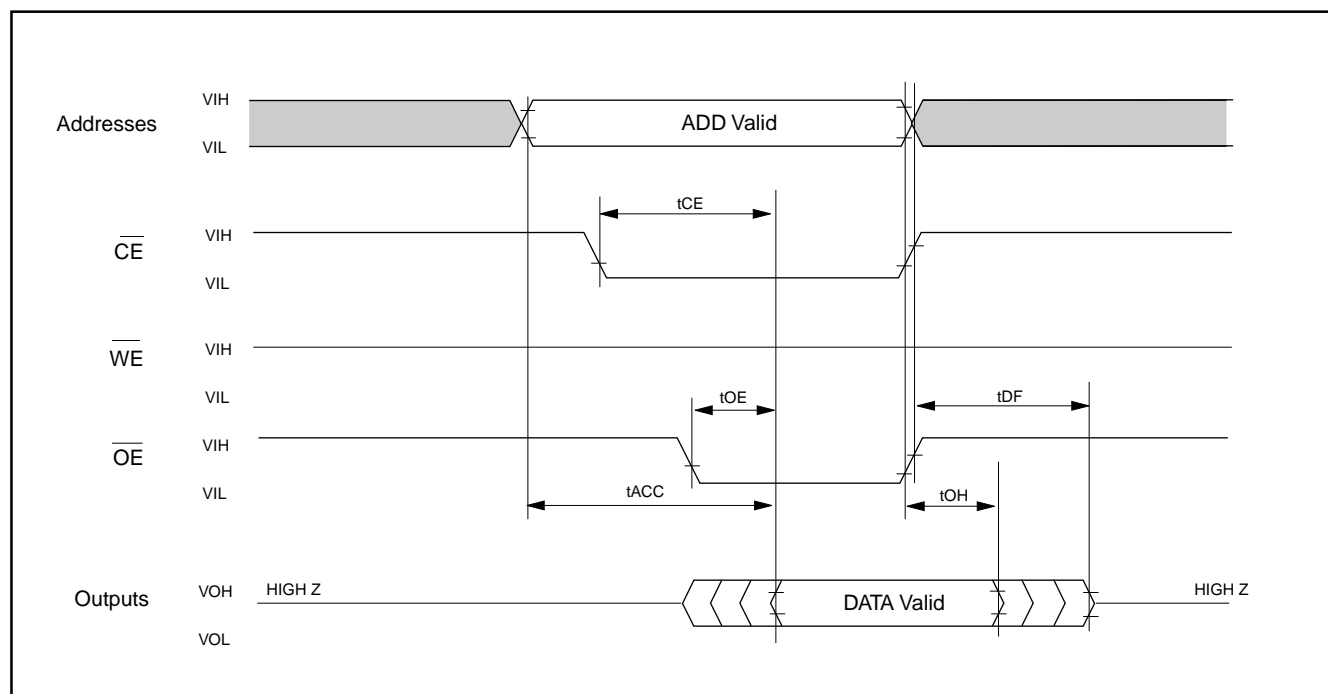
COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS TA = 0°C TO 70°C, -40°C TO 125°C(Note 5), VCC = 5V±10%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=1MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	$\overline{CE}$=VIH, Erase Suspended

NOTES:
1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guaranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.
5. The automotive grade is under development.

AC CHARACTERISTICS TA = 0°C TO 70°C, -40°C TO 125°C(Note), VCC = 5V±10%

SYMBOL	PARAMETER	29F800T/B-70		29F800T/B-90		29F800T/B-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tOES	$\overline{OE}$ setup time	35		35		35		ns
tCWC	Command programming cycle	70		90		120		ns
tCEP	$\overline{WE}$ programming pulse width	55		55		55		ns
tCEPH1	$\overline{WE}$ programming pulse width High	20		20		20		ns
tCEPH2	$\overline{WE}$ programming pulse width High	20		20		20		ns
tAS	Address setup time	0		0		0		ns
tAH	Address hold time	45		45		50		ns
tDS	Data setup time	35		45		50		ns
tDH	Data hold time	0		0		0		ns
tCESC	$\overline{CE}$ setup time before command write	0		0		0		ns
tAETC	Total erase time in auto chip erase	13(TYP.)	35	13(TYP.)	35	13(TYP.)	35	s
tAETB	Total erase time in auto sector erase	3(TYP.)	12	3(TYP.)	12	3(TYP.)	12	s
tAVT	Total programming time in auto verify (byte/word program time)	7/12(TYP.)	210/360	7/12(TYP.)	210/360	7/12(TYP.)	210/360	us
tBAL	Sector address load time	100		100		100		us
tCH	$\overline{CE}$ Hold Time	0		0		0		ns
tCS	$\overline{CE}$ setup to $\overline{WE}$ going low	0		0		0		ns
tVLHT	Voltage Transition Time	4		4		4		us
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		4		4		us
tWPP1	Write pulse width for sector protect	10		10		10		us
tWPP2	Write pulse width for sector unprotect	12		12		12		ms

Note: The automotive grade is under development.

SWITCHING TEST CIRCUITS

CL=100pF Including jig capacitance for MX29F800T/B-90 & MX29F800T/B-12.
CL=30pF Including jig capacitance for MX29F800T/B-70.
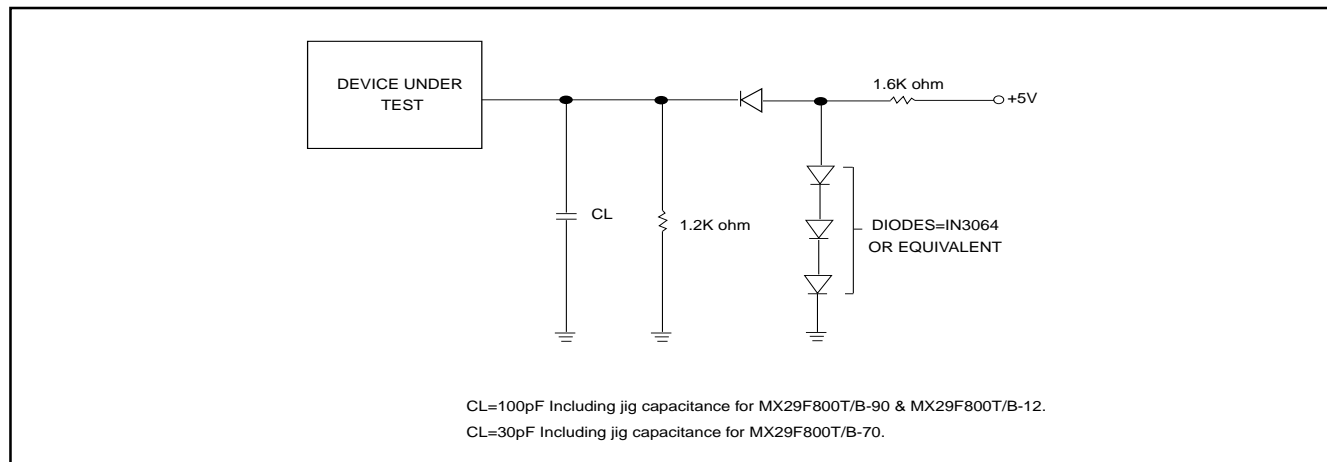
SWITCHING TEST WAVEFORMS

AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are <20ns.
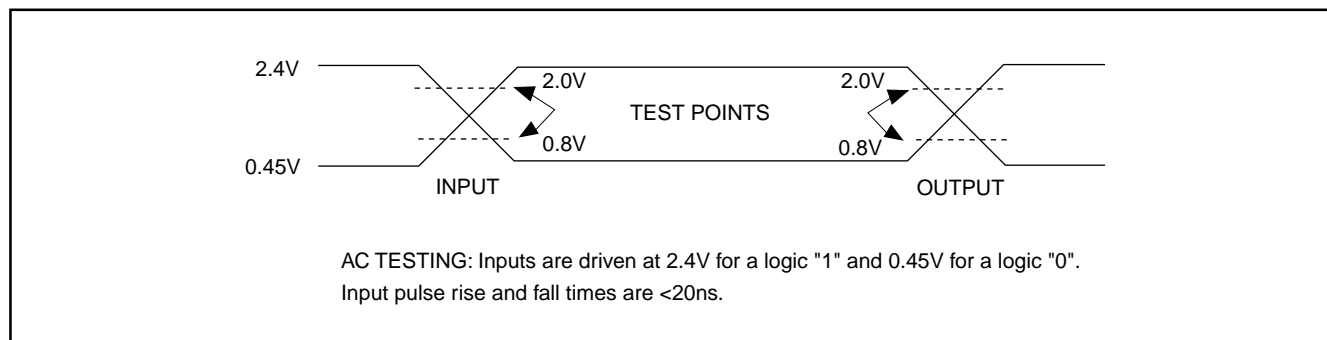
COMMAND WRITE TIMING WAVEFORM
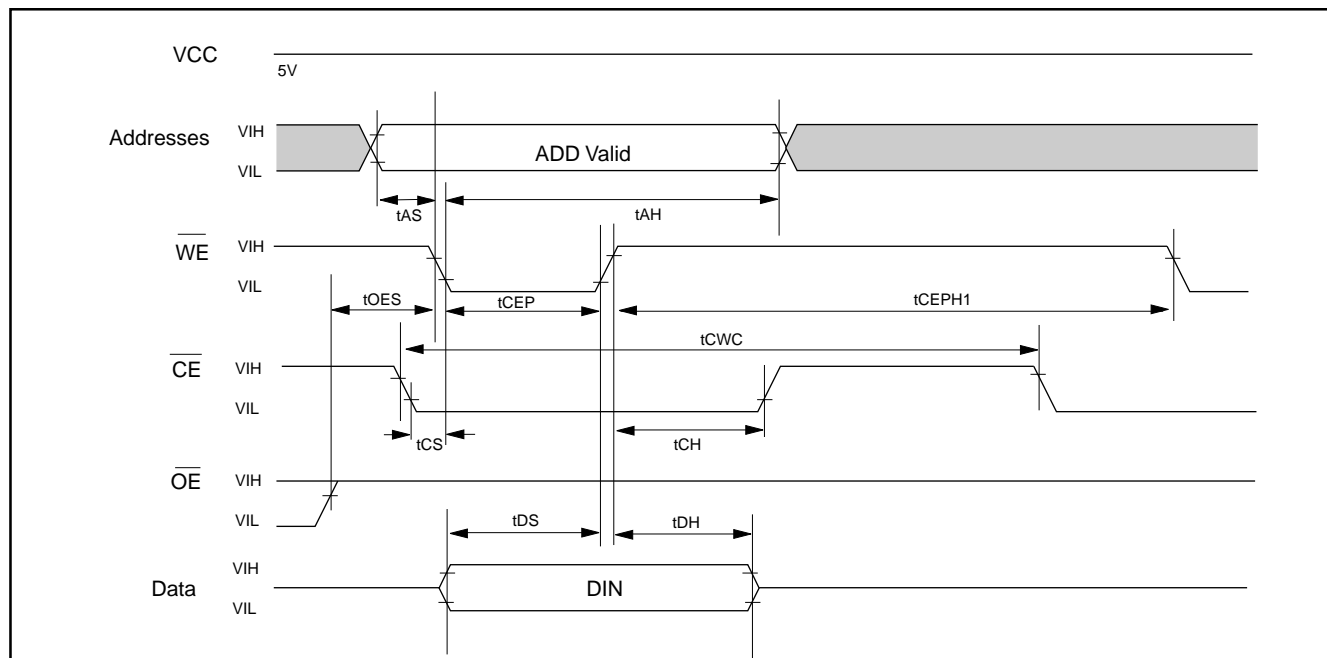
AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic verification starts. Device outputs $\overline{DATA}$ during programming and DATA after programming on Q7. (Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

AUTOMATIC PROGRAMMING TIMING WAVEFORM (WORD MODE)

Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit
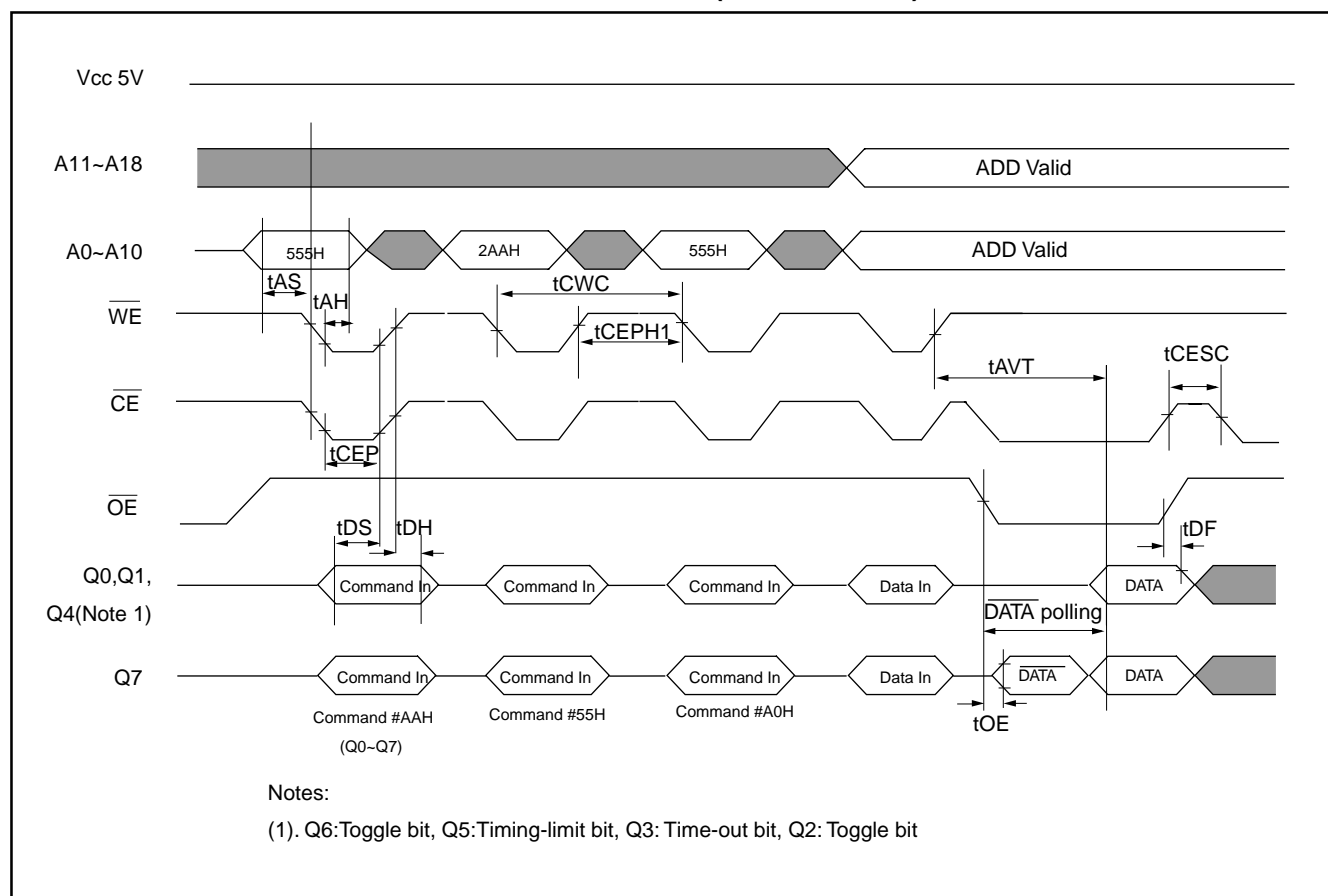
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART (WORD MODE)
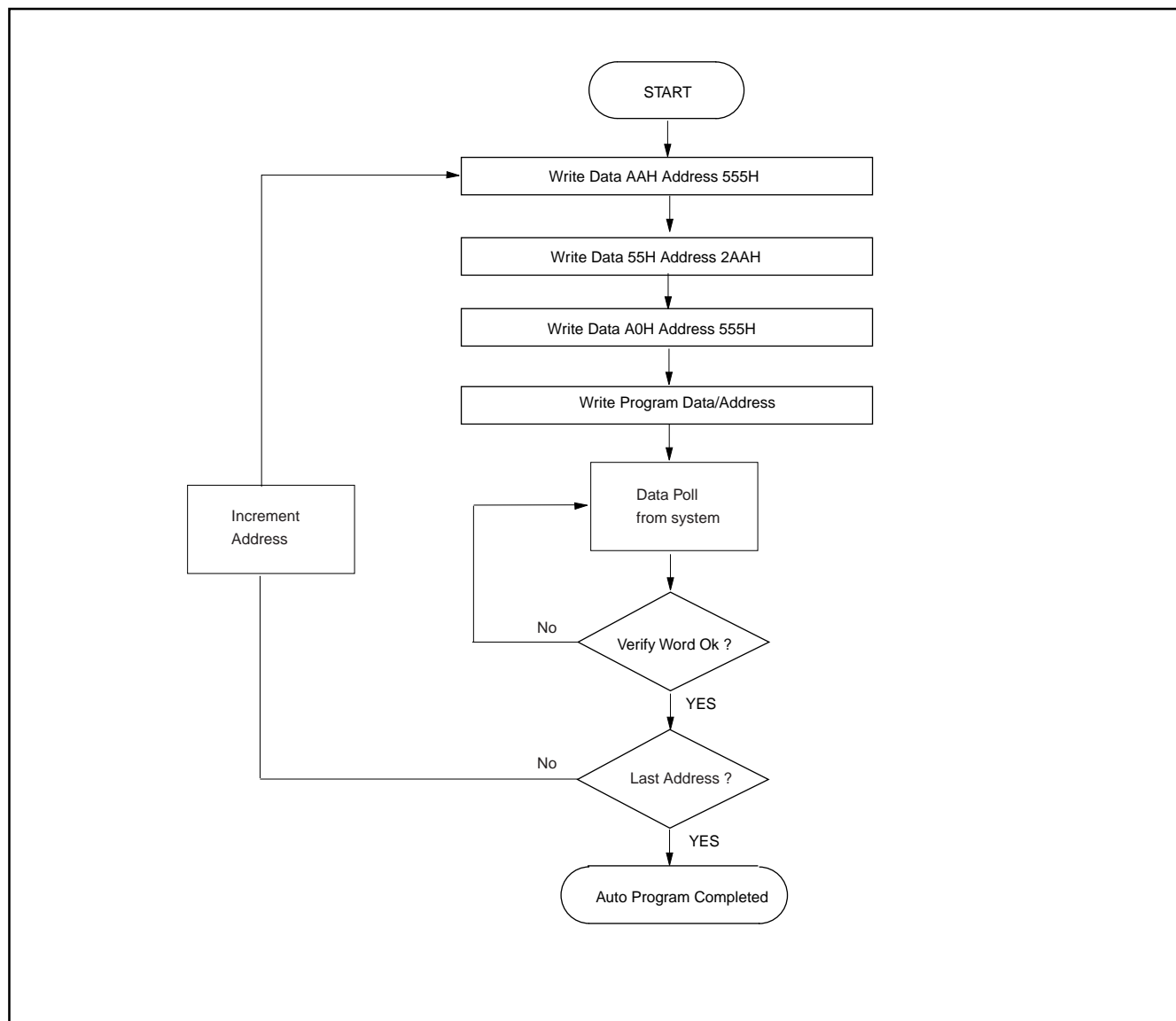
AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

AUTOMATIC CHIP ERASE TIMING WAVEFORM (WORD MODE)

Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART (WORD MODE)

```
                    START

         Write Data AAH Address 555H

         Write Data 55H Address 2AAH

         Write Data 80H Address 555H

         Write Data AAH Address 555H

         Write Data 55H Address 2AAH

         Write Data 10H Address 555H

              Data Poll
             from system
                              YES

   No       DATA = FFh ?

                              YES

          Auto Erase Completed
```

AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector data indicated by A12 to A18 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by $\overline{DATA}$ polling and toggle bit check-ing after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

AUTOMATIC SECTOR ERASE TIMING WAVEFORM (WORD MODE)

Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART (WORD MODE)

```
                    ┌──────────┐
                    │  START   │
                    └────┬─────┘
                         ▼
          ┌──────────────────────────────┐
          │  Write Data AAH Address 555H  │
          └───────────────┬──────────────┘
                          ▼
          ┌──────────────────────────────┐
          │  Write Data 55H Address 2AAH  │
          └───────────────┬──────────────┘
                          ▼
          ┌──────────────────────────────┐
          │  Write Data 80H Address 555H  │
          └───────────────┬──────────────┘
                          ▼
          ┌──────────────────────────────┐
          │  Write Data AAH Address 555H  │
          └───────────────┬──────────────┘
                          ▼
          ┌──────────────────────────────┐
          │  Write Data 55H Address 2AAH  │
          └───────────────┬──────────────┘
                          ▼
          ┌──────────────────────────────┐
          │  Write Data 30H Sector Address │◄──────┐
          └───────────────┬──────────────┘        │
                          ▼                         │
                    ╱           ╲      NO           │
                   ╱  Last Sector ╲─────────────────┘
                   ╲  to Erase ?  ╱
                    ╲           ╱
                       │ YES
                       ▼
          ┌──────────────────────────────┐
          │     Data Poll from System     │◄──────┐
          └───────────────┬──────────────┘        │
                          ▼                         │
                    ╱           ╲      NO           │
                   ╱  Data=FFh?   ╲─────────────────┘
                    ╲           ╱
                       │ YES
                       ▼
             ┌─────────────────────────┐
             │ Auto Sector Erase Completed │
             └─────────────────────────┘
```
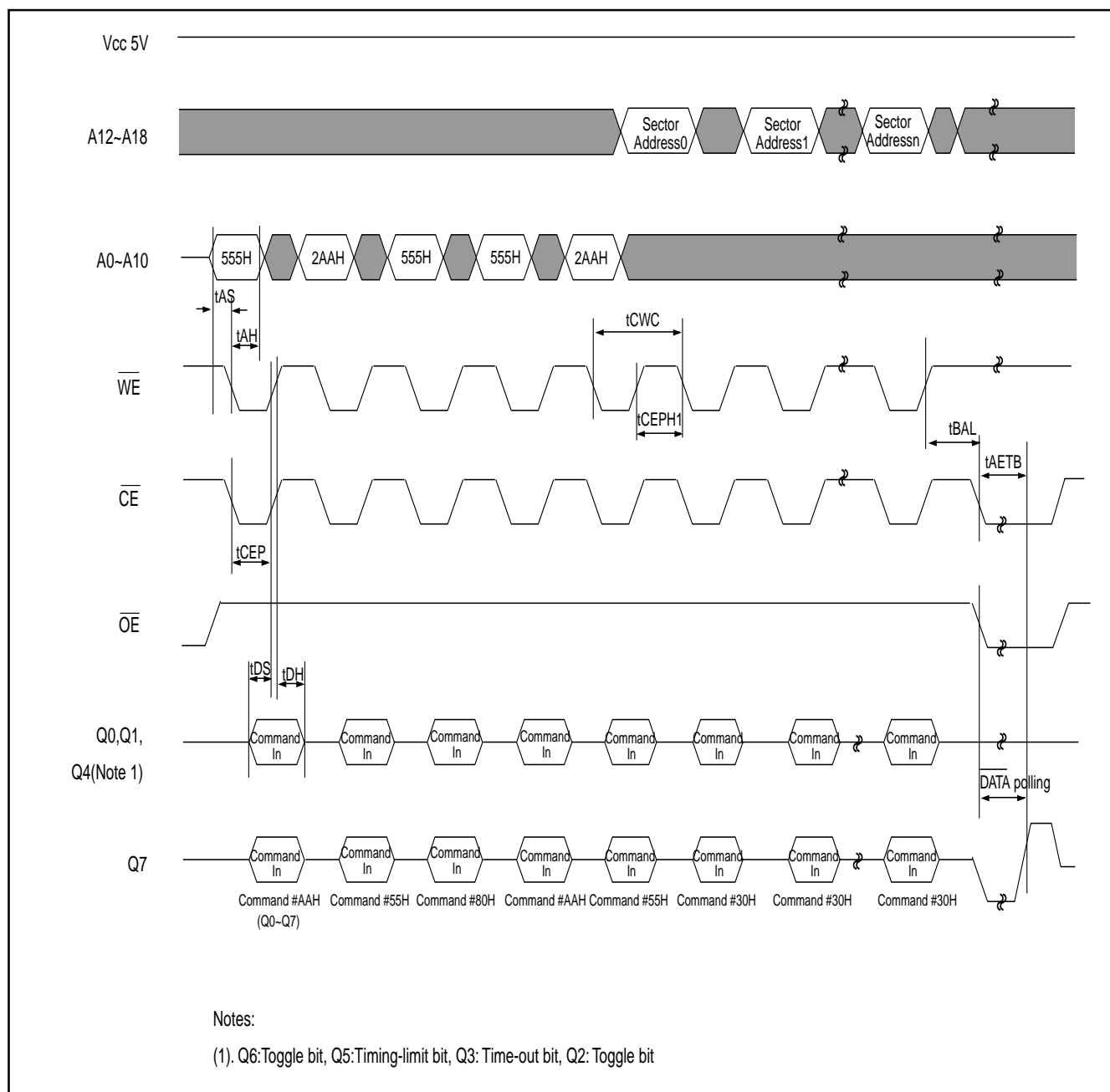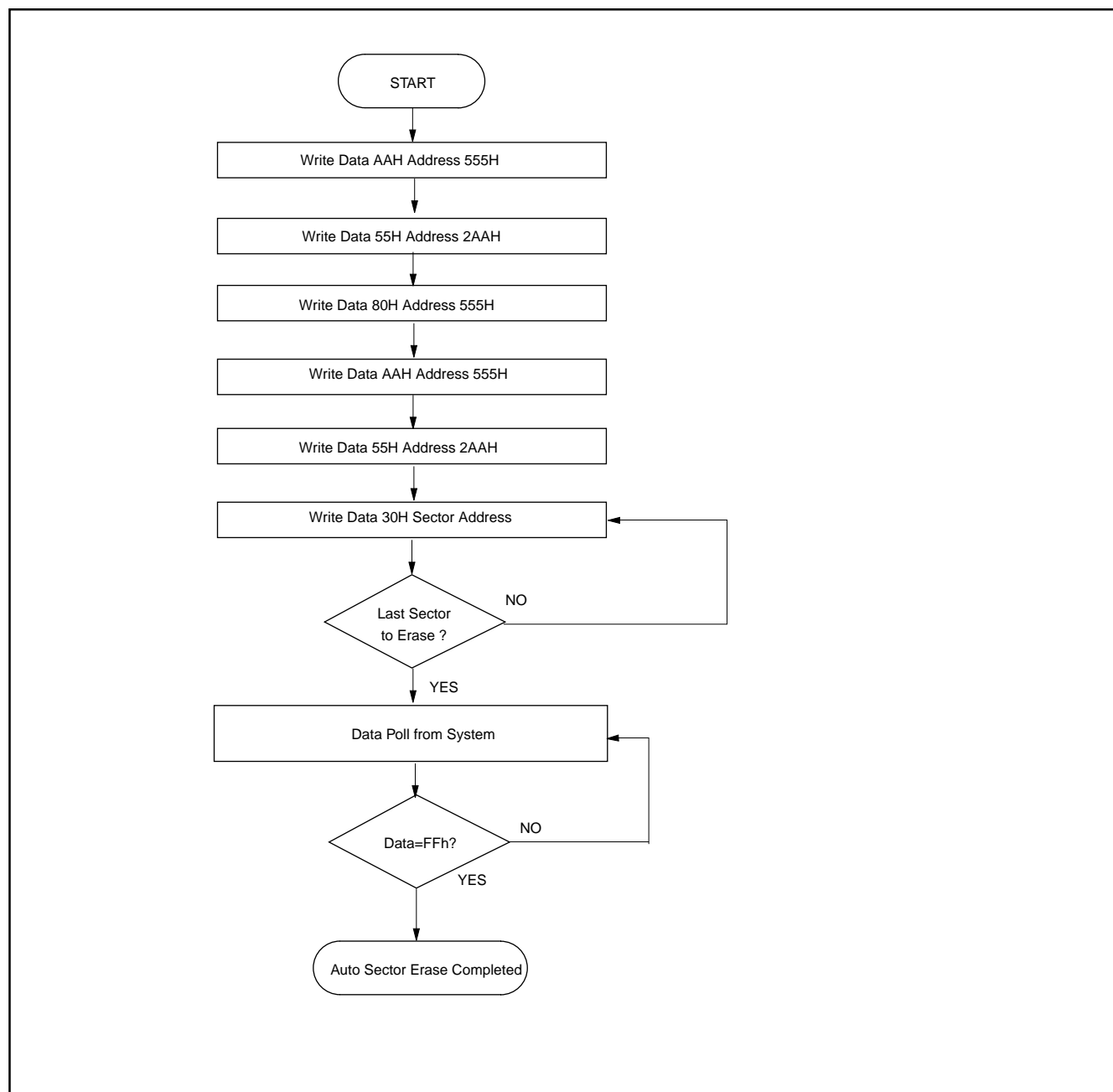
ERASE SUSPEND/ERASE RESUME FLOWCHART

```
                    ┌─────────┐
                    │  START  │
                    └────┬────┘
                         │
                  ┌──────▼──────┐
                  │ Write Data B0H │
                  └──────┬──────┘
                         │            ◄──────┐
                         ▼                   │
                    ╱─────────╲              │
                   ╱ Toggle Bit ╲   NO        │
                  ╱ checking Q6   ╲───────────┘
                  ╲ not toggled   ╱
                   ╲─────────────╱
                         │ YES
                         ▼
                  ┌─────────────┐
                  │ Read Array or │  ◄──────┐
                  │   Program    │          │
                  └──────┬──────┘           │
                         ▼                  │
                    ╱─────────╲             │
                   ╱ Reading or ╲   NO        │
                  ╱ Programming End ╲─────────┘
                   ╲─────────────╱
                         │ YES
                         ▼
                  ┌─────────────┐
                  │ Write Data 30H │
                  └──────┬──────┘
                         ▼
                  ┌─────────────┐
                  │ Continue Erase │  ◄──────┐
                  └──────┬──────┘           │
                         ▼                  │
                    ╱─────────╲             │
                   ╱  Another   ╲   NO        │
                  ╱ Erase Suspend? ╲─────────┘
                   ╲─────────────╱
                         │ YES
```
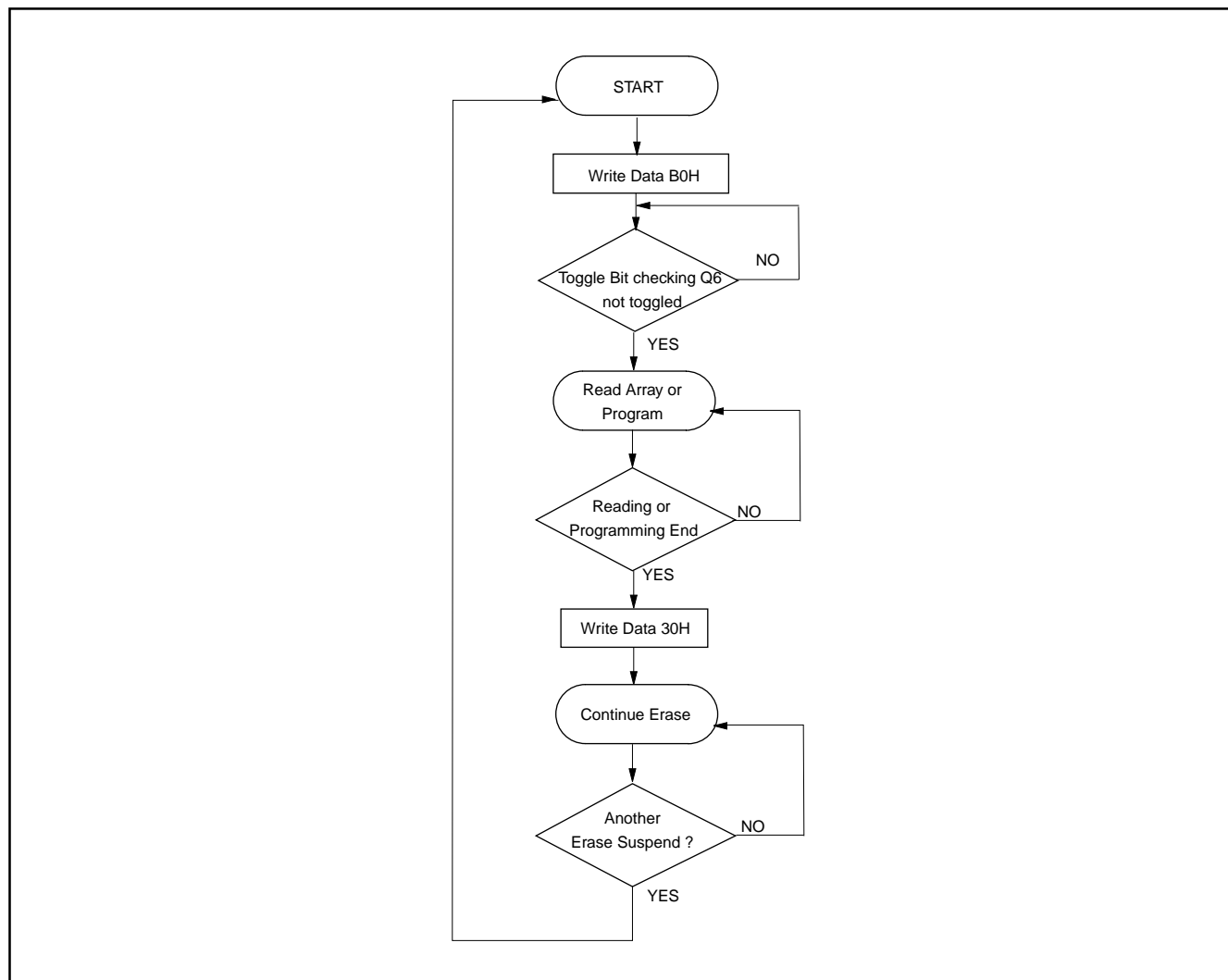
TIMING WAVEFORM FOR SECTOR PROTECTION
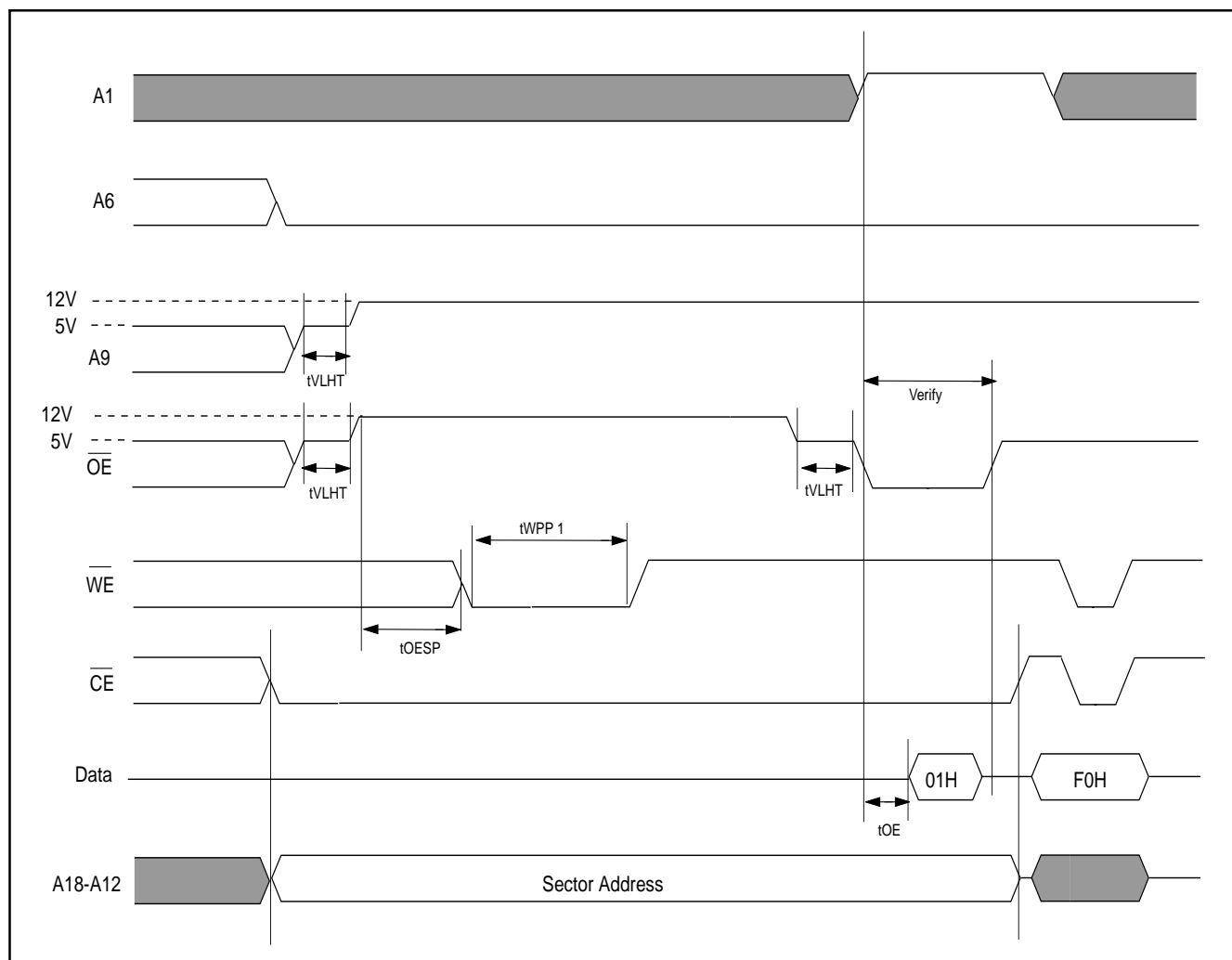
TIMING WAVEFORM FOR CHIP UNPROTECTION

SECTOR PROTECTION ALGORITHM

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                           ▼
              ┌──────────────────────────┐◄──────────────┐
              │    Set Up Sector Addr    │               │
              │ (A18,A16,A15,A14,A13,A12)│               │
              └────────────┬─────────────┘               │
                           │                             │
                           ▼                             │
              ┌──────────────────────────┐               │
              │         PLSCNT=1         │               │
              └────────────┬─────────────┘               │
                           │                             │
                           ▼                             │
              ┌──────────────────────────┐               │
      ┌──────►│  OE=VID,A9=VID,CE=VIL    │               │
      │       │         A6=VIL           │               │
      │       └────────────┬─────────────┘               │
      │                    │                             │
      │                    ▼                             │
      │       ┌──────────────────────────┐               │
      │       │     Activate WE Pulse    │               │
      │       └────────────┬─────────────┘               │
      │                    │                             │
      │                    ▼                             │
      │       ┌──────────────────────────┐               │
      │       │       Time Out 10us      │               │
      │       └────────────┬─────────────┘               │
      │                    │                             │
      │                    ▼                             │
      │       ┌──────────────────────────┐               │
      │       │  Set WE=VIH, CE=OE=VIL   │               │
      │       │   A9 should remain VID   │               │
      │       └────────────┬─────────────┘               │
      │                    │                             │
      │                    ▼                             │
      │       ┌──────────────────────────┐               │
      │       │      Read from Sector    │               │
      │       │       Addr=SA, A1=1      │               │
      │       └────────────┬─────────────┘               │
 No   │                    │                             │
      │                    ▼                             │
   ◇─────◇      No    ◇──────────◇                       │
  ◇PLSCNT=◇◄──────────◇ Data=01H? ◇                      │
  ◇ 32?   ◇           ◇──────────◇                       │
   ◇─────◇                 │ Yes                         │
      │ Yes                ▼                             │
      ▼              ◇──────────◇         Yes            │
┌───────────┐       ◇  Protect   ◇────────────────────── ┘
│  Device   │       ◇  Another   ◇
│  Failed   │       ◇  Sector?   ◇
└───────────┘        ◇──────────◇
                          │ No
                          ▼
              ┌──────────────────────────┐
              │    Remove VID from A9    │
              │   Write Reset Command    │
              └────────────┬─────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │Sector Protection│
                    │   Complete   │
                    └─────────────┘
```

CHIP UNPROTECTION ALGORITHM

```
                              ┌─────────────┐
                              │    START    │
                              └─────────────┘
                                     │
                              ┌──────────────────┐
                              │ Protect All Sectors │
                              └──────────────────┘
                                     │
                              ┌──────────────────┐
                              │     PLSCNT=1      │
                              └──────────────────┘
                                     │
                              ┌──────────────────┐
                              │ Set OE=A9=VID    │◄──────────────┐
                              │ CE=VIL,A6=1      │               │
                              └──────────────────┘               │
                                     │                           │
                              ┌──────────────────┐               │
                              │ Activate WE Pulse │               │
                              └──────────────────┘               │
                                     │                   ┌──────────────┐
                              ┌──────────────────┐        │  Increment   │
                              │  Time Out 12ms   │        │   PLSCNT     │
                              └──────────────────┘        └──────────────┘
                                     │                           ▲
                              ┌──────────────────┐               │
                              │ Set OE=CE=VIL    │               │ No
                              │ A9=VID,A1=1      │               │
                              └──────────────────┘               │
                                     │                           │
                              ┌──────────────────┐               │
                              │ Set Up First Sector Addr │        │
                              └──────────────────┘               │
                                     │                           │
      ┌─────────────┐         ┌──────────────────┐               │
      │  Increment  │────────►│ Read Data from Device │           │
      │ Sector Addr │         └──────────────────┘               │
      └─────────────┘                │                    ┌──────────────┐
             ▲                   ╱───────╲      No         ╱───────────╲
             │                  ╱ Data=00H? ╲─────────────►  PLSCNT=1000? 
             │ No               ╲───────────╱              ╲───────────╱
             │                       │ Yes                       │ Yes
             │                   ╱───────────╲             ┌──────────────┐
             └──────────────────╱ All sectors ╲            │ Device Failed │
                                ╲ been verified?╱           └──────────────┘
                                 ╲─────────────╱
                                      │ Yes
                              ┌──────────────────┐
                              │ Remove VID from A9 │
                              │ Write Reset Command│
                              └──────────────────┘
                                     │
                              ┌─────────────┐
                              │ Chip Unprotect │
                              │   Complete   │
                              └─────────────┘
```

* It is recommended before unprotect whole chip, all sectors should be protected in advance.

AC CHARACTERISTICS

Parameter Std	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	RESET Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	RESET Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET High Time Before Read (See Note)	MIN	0	ns
tRB1	RY/BY Recovery Time (to CE, OE go low)	MIN	0	ns
tRB2	RY/BY Recovery Time (to WE go low)	MIN	50	ns

Note:Not 100% tested

RESET TIMING WAVEFORM

Reset Timing NOT during Automatic Algorithms

Reset Timing during Automatic Algorithms
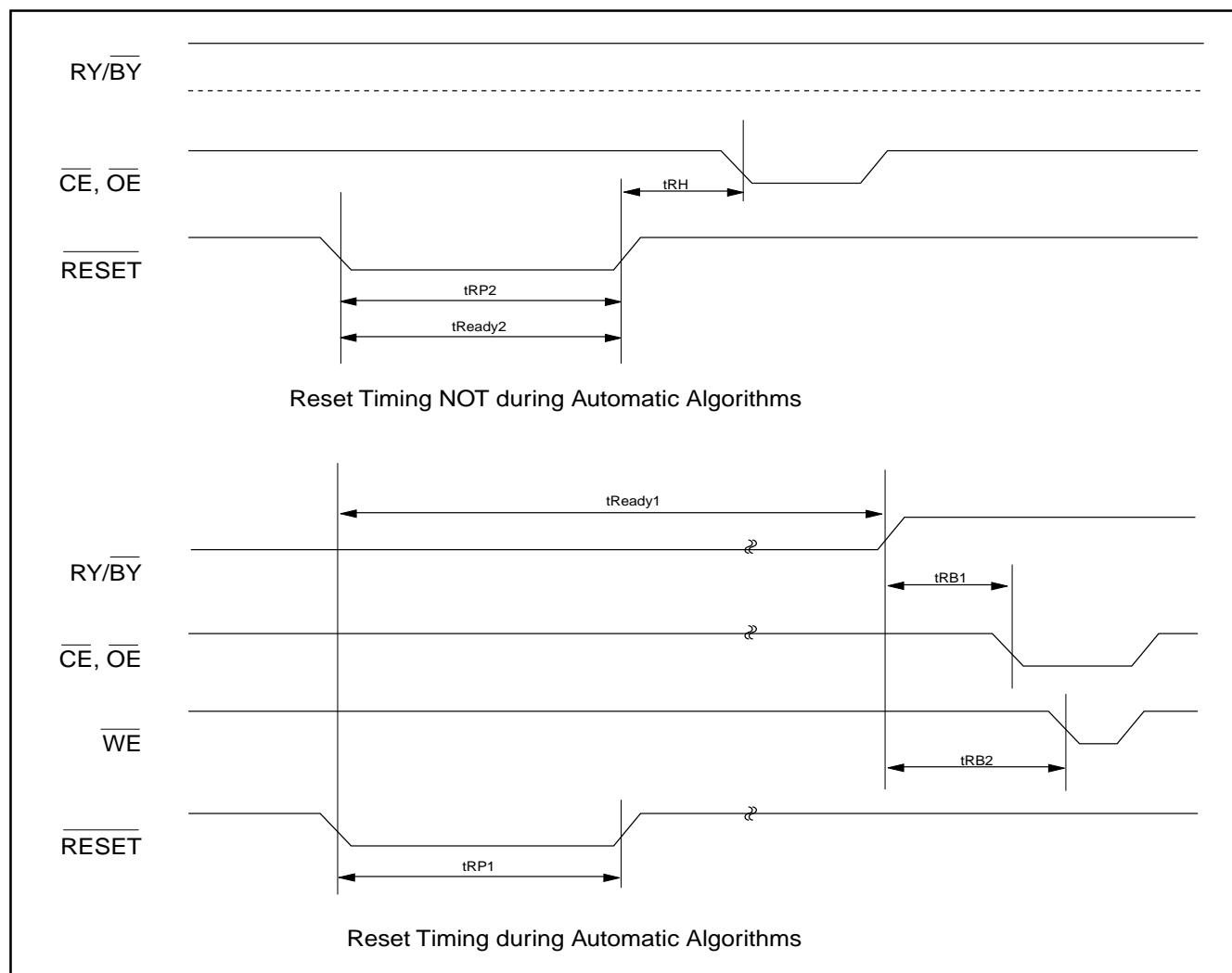
TEMPORARY SECTOR UNPROTECT

Parameter Std.	Description	Test Setup	All Speed Options	Unit
tVIDR	VID Rise and Fall Time (See Note)	Min	500	ns
tRSP	$\overline{RESET}$ Setup Time for Temporary Sector Unprotect	Min	4	us

Note:
Not 100% tested

TEMPORARY SECTOR UNPROTECT TIMING DIAGRAM

TEMPORARY SECTOR UNPROTECT ALGORITHM

Start

$\overline{\text{RESET}}$ = VID (Note 1)

Perform Erase or Program Operation

Operation Completed

$\overline{\text{RESET}}$ = VIH
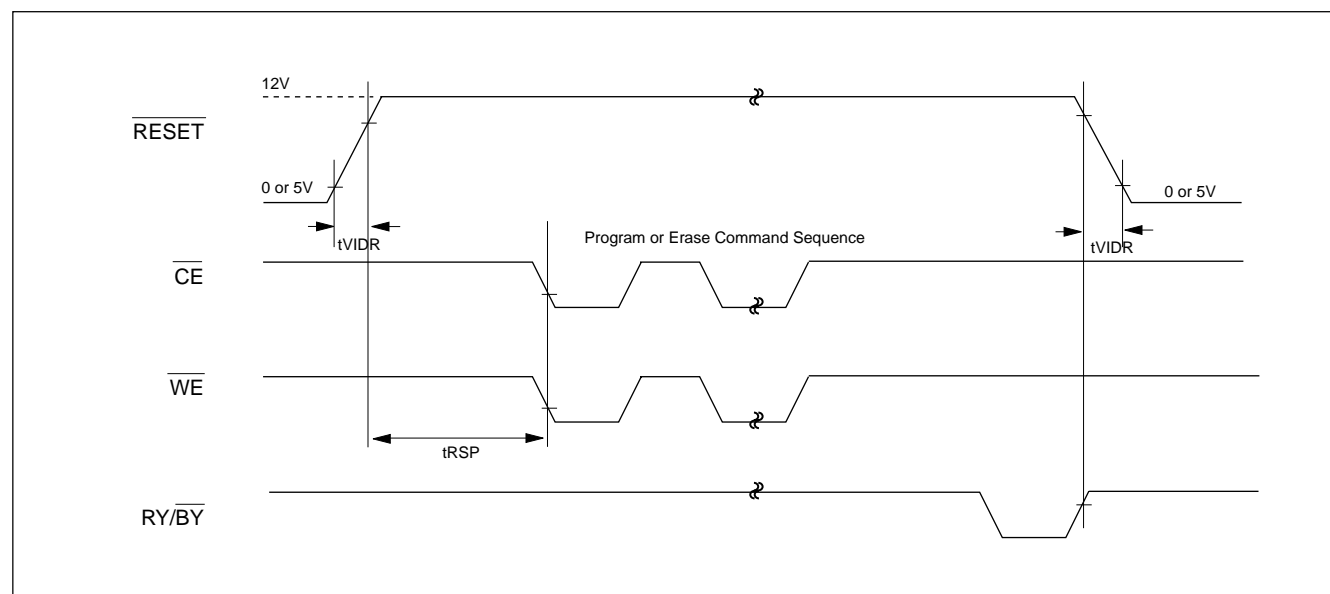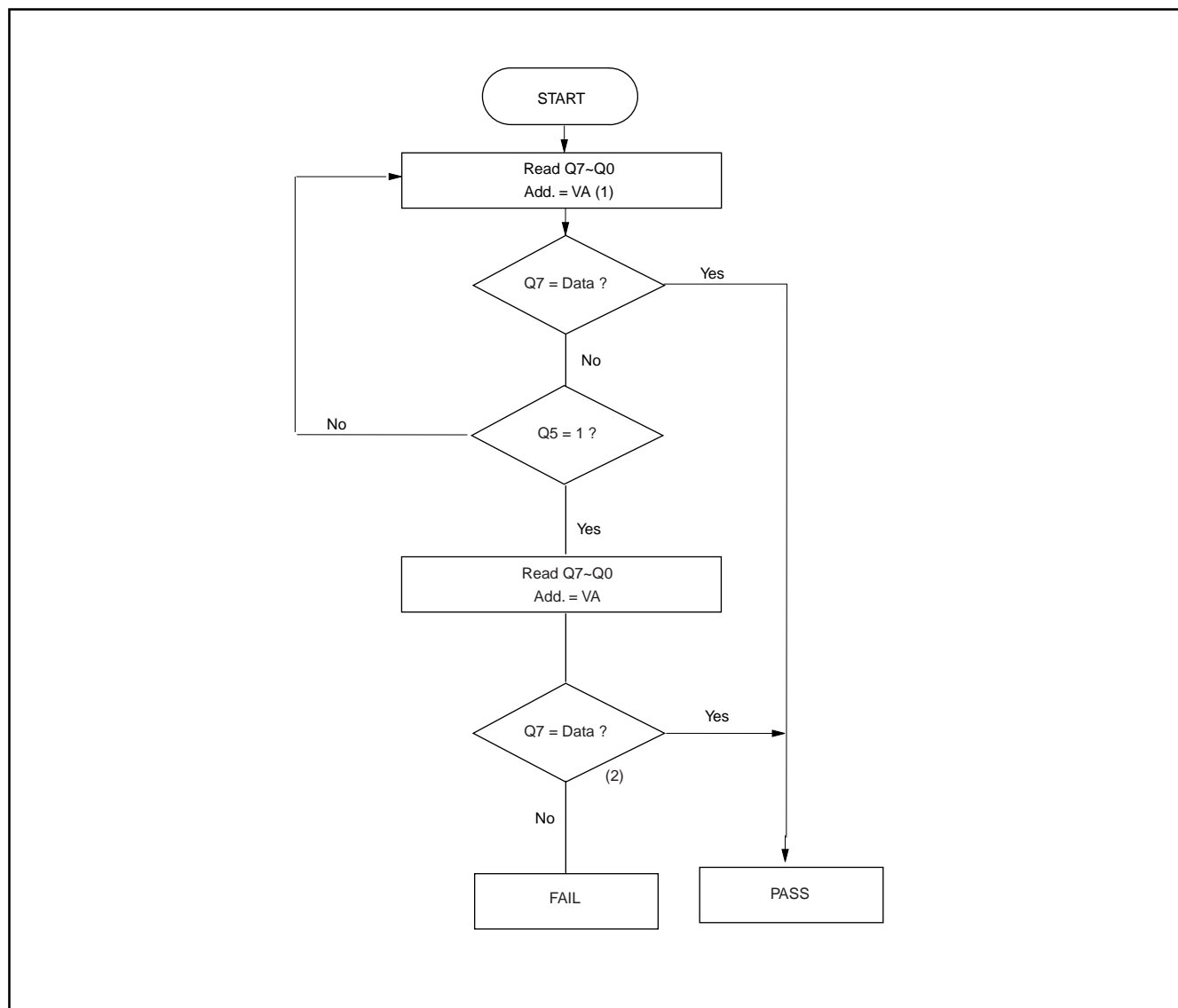
Temporary Sector Unprotect Completed(Note 2)
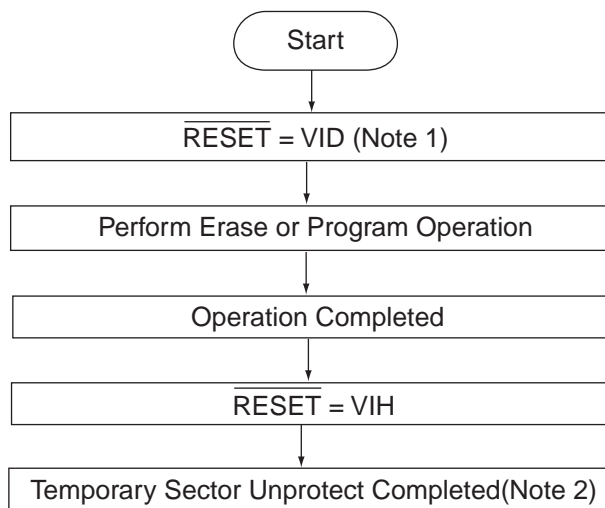
Note : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V

2. All previously protected sectors are protected again.

## DATA POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

NOTES:

VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data raed cycle.

DATA POLLING ALGORITHM

```
                        ┌─────────┐
                        │  START  │
                        └────┬────┘
                             │
            ┌───────►┌───────────────┐
            │        │  Read Q7~Q0   │
            │        │  Add. = VA (1)│
            │        └───────┬───────┘
            │                │
            │           ╱─────────╲
            │          ╱           ╲      Yes
            │         ╱  Q7 = Data ? ╲────────────┐
            │         ╲             ╱              │
            │          ╲           ╱               │
            │           ╲─────────╱                │
            │                │ No                  │
            │                │                     │
            │           ╱─────────╲                │
      No    │          ╱           ╲               │
     ◄──────┤         ╱   Q5 = 1 ?  ╲              │
            │         ╲             ╱              │
            │          ╲           ╱               │
            │           ╲─────────╱                │
            │                │ Yes                 │
            │                │                     │
            │        ┌───────────────┐             │
            │        │  Read Q7~Q0   │             │
            │        │   Add. = VA   │             │
            │        └───────┬───────┘             │
            │                │                     │
            │           ╱─────────╲                │
            │          ╱           ╲      Yes       │
            │         ╱  Q7 = Data ? ╲──────────┐   │
            │         ╲             ╱           │   │
            │          ╲           ╱ (2)        │   │
            │           ╲─────────╱             │   │
            │                │ No               │   │
            │                │                  ▼   │
            │        ┌───────────────┐    ┌──────────┐
            │        │     FAIL      │    │   PASS   │
            │        └───────────────┘    └──────────┘
```
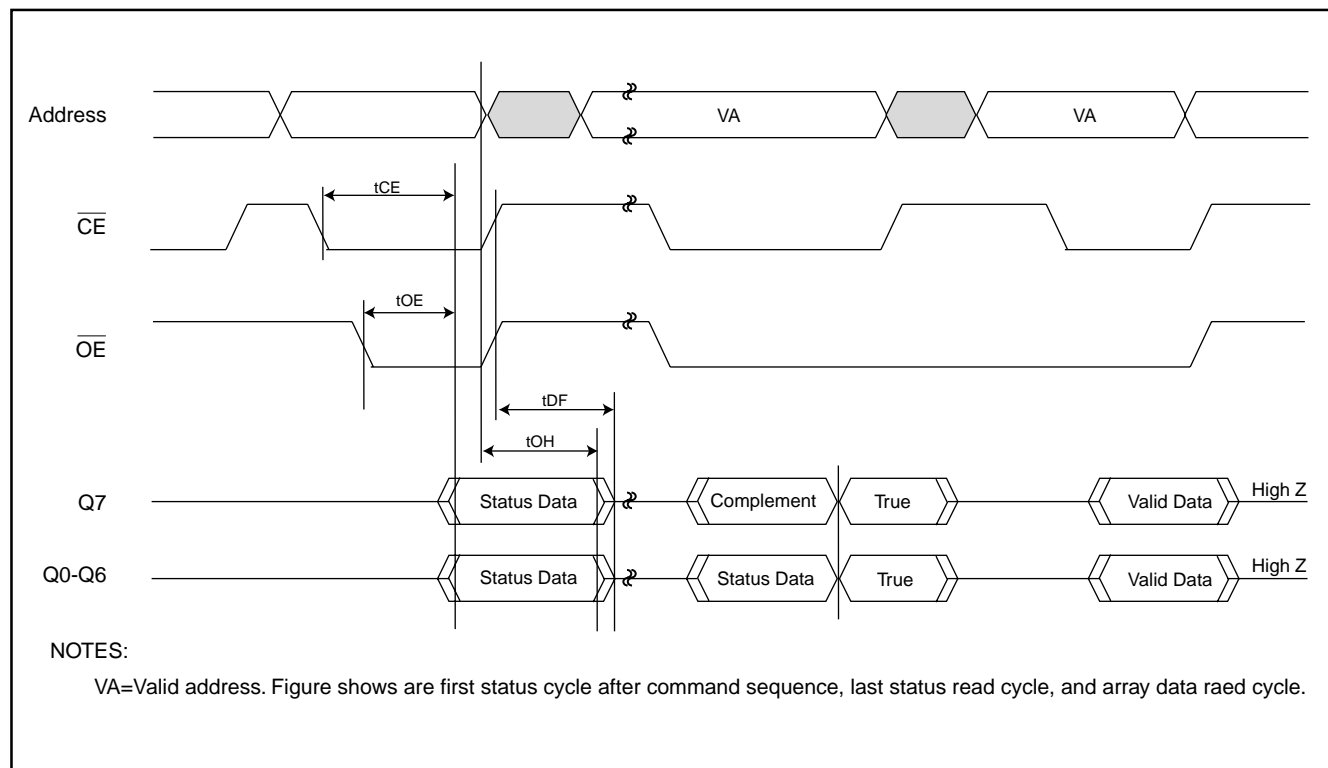
Notes:
1. VA=valid address for programming.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)
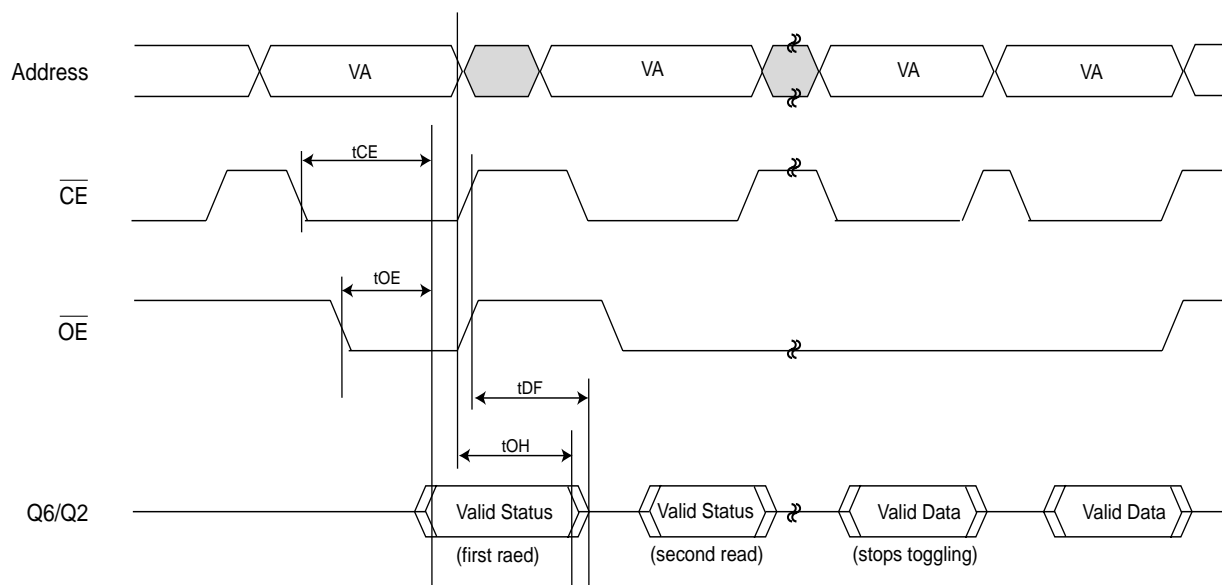
NOTES:

VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.
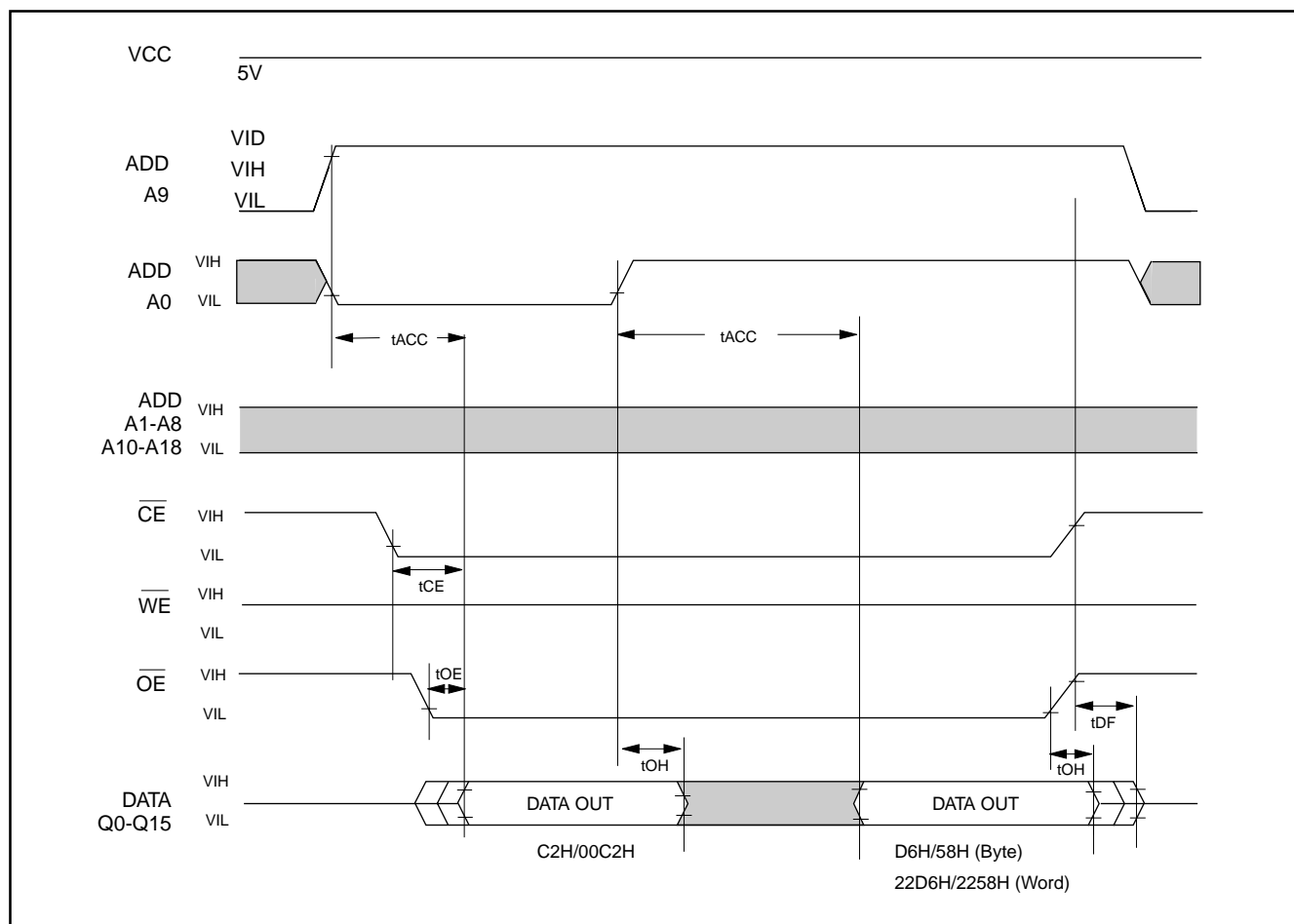
TOGGLE BIT ALGORITHM
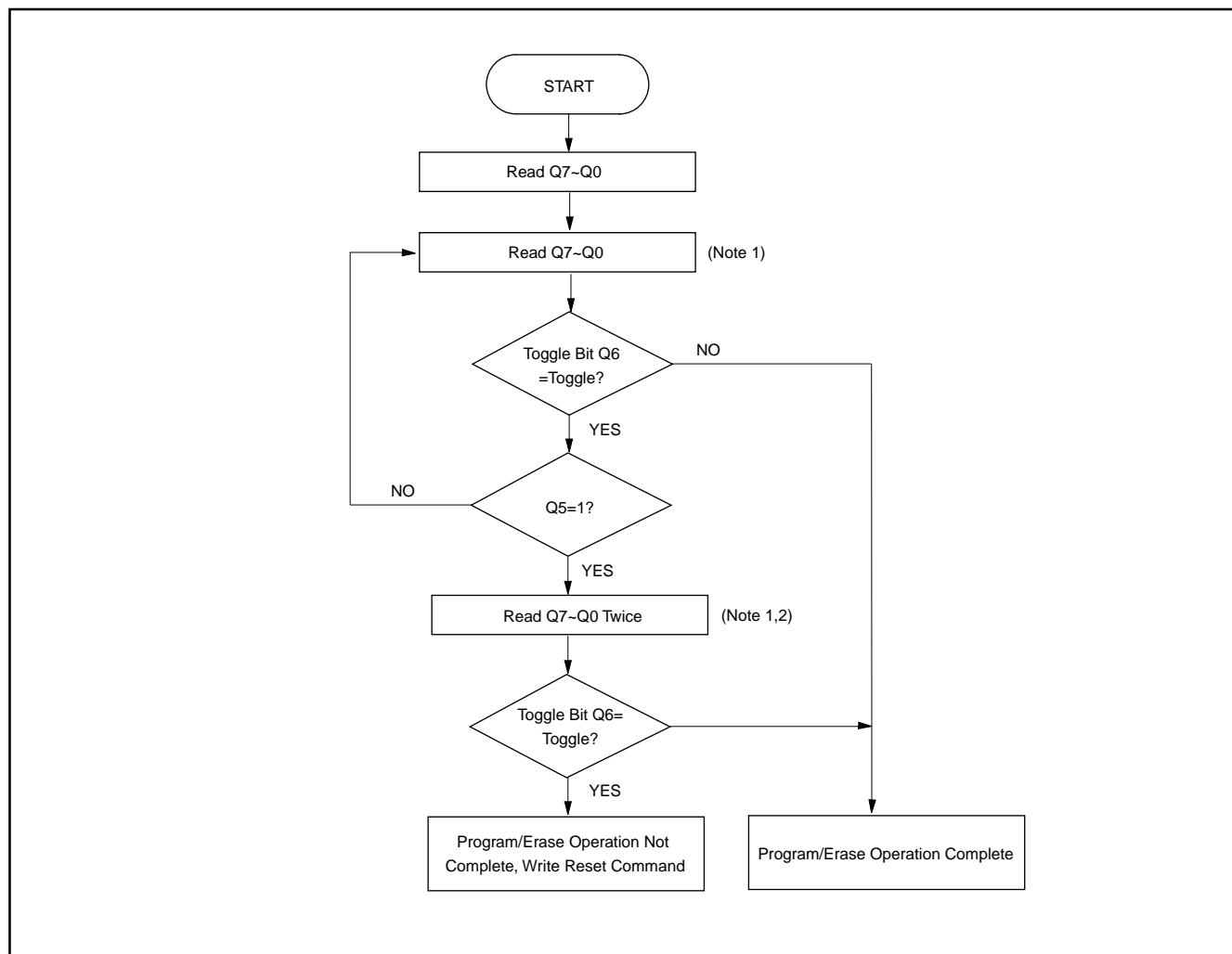
Note:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

ID CODE READ TIMING WAVEFORM

ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	MIN.	LIMITS TYP.(2)	MAX.(3)	UNITS
Sector Erase Time		3	12	sec
Chip Erase Time		13	35	sec
Byte Programming Time		7	210	us
Word Programming Time		12	360	us
Chip Programming Time		8	24	sec
Erase/Program Cycles	100,000			Cycles

Note: 1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25°C, 5V.
3. Maximum values measured at 25°C, 4.5V.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

ORDERING INFORMATION

PART NO.	Access Time (ns)	Operating Current MAX.(mA)	Standby Current MAX.(uA)	Package	Remark
MX29F800TMC-70	70	50	5	44 Pin SOP	
MX29F800TMC-90	90	50	5	44 Pin SOP	
MX29F800TMC-12	120	50	5	44 Pin SOP	
MX29F800TTC-70	70	50	5	48 Pin TSOP (Normal Type)	
MX29F800TTC-90	90	50	5	48 Pin TSOP (Normal Type)	
MX29F800TTC-12	120	50	5	48 Pin TSOP (Normal Type)	
* MX29F800TTA-90	90	50	20	48 Pin TSOP (Normal Type)	
* MX29F800TTA-12	120	50	20	48 Pin TSOP (Normal Type)	
MX29F800TTC-70G	70	50	5	48 Pin TSOP (Normal Type)	PB free
MX29F800TTC-90G	90	50	5	48 Pin TSOP (Normal Type)	PB free
MX29F800TTC-12G	120	50	5	48 Pin TSOP (Normal Type)	PB free
* MX29F800BTA-90	90	50	20	48 Pin TSOP (Normal Type)	
* MX29F800BTA-12	120	50	20	48 Pin TSOP (Normal Type)	
MX29F800BMC-70	70	50	5	44 Pin SOP	
MX29F800BMC-90	90	50	5	44 Pin SOP	
MX29F800BMC-12	120	50	5	44 Pin SOP	
MX29F800BTC-70	70	50	5	48 Pin TSOP (Normal Type)	
MX29F800BTC-90	90	50	5	48 Pin TSOP (Normal Type)	
MX29F800BTC-12	120	50	5	48 Pin TSOP (Normal Type)	
MX29F800BTC-70G	70	50	5	48 Pin TSOP (Normal Type)	PB free
MX29F800BTC-90G	90	50	5	48 Pin TSOP (Normal Type)	PB free
MX29F800BTC-12G	120	50	5	48 Pin TSOP (Normal Type)	PB free

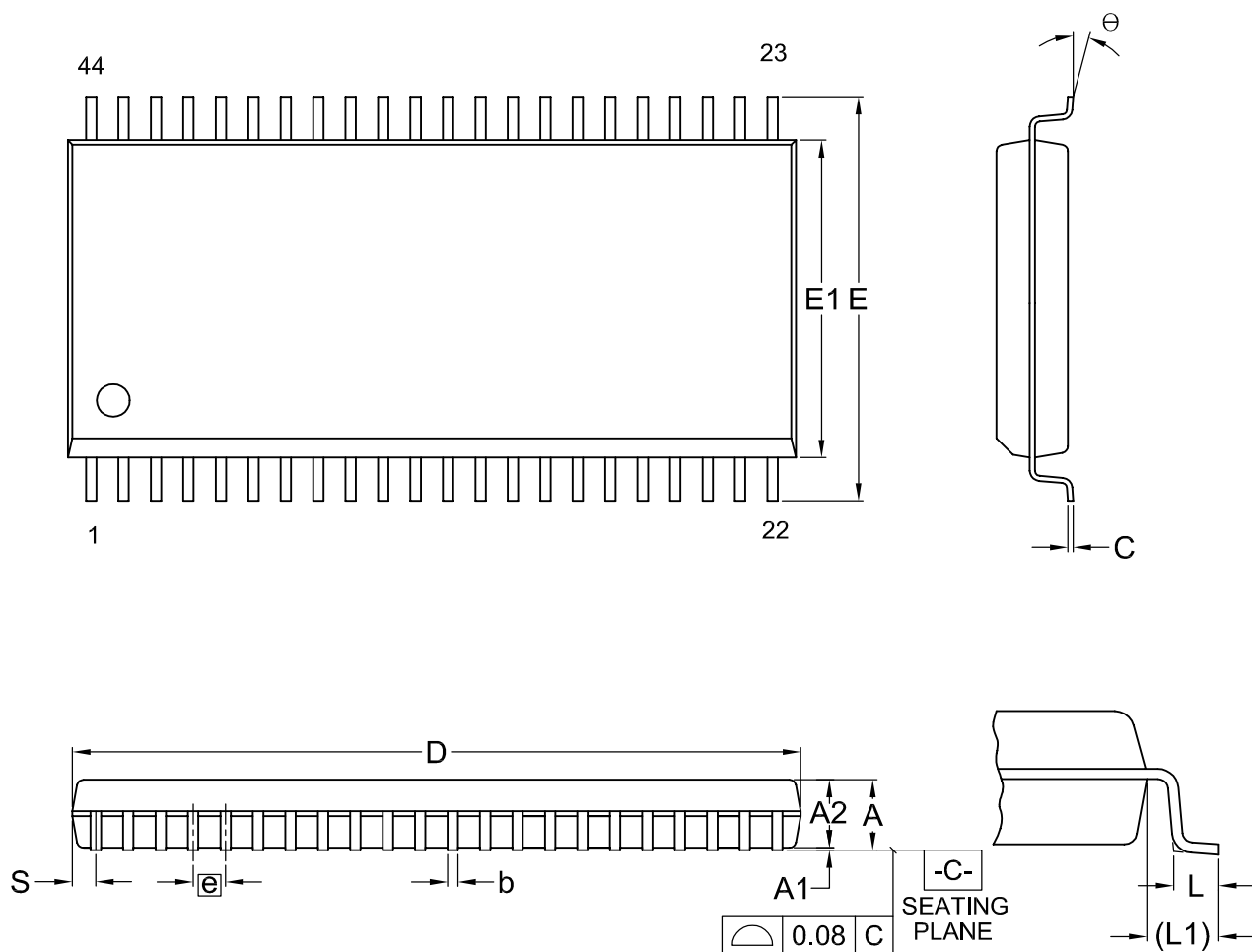* The automotive grade is under development.

PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM
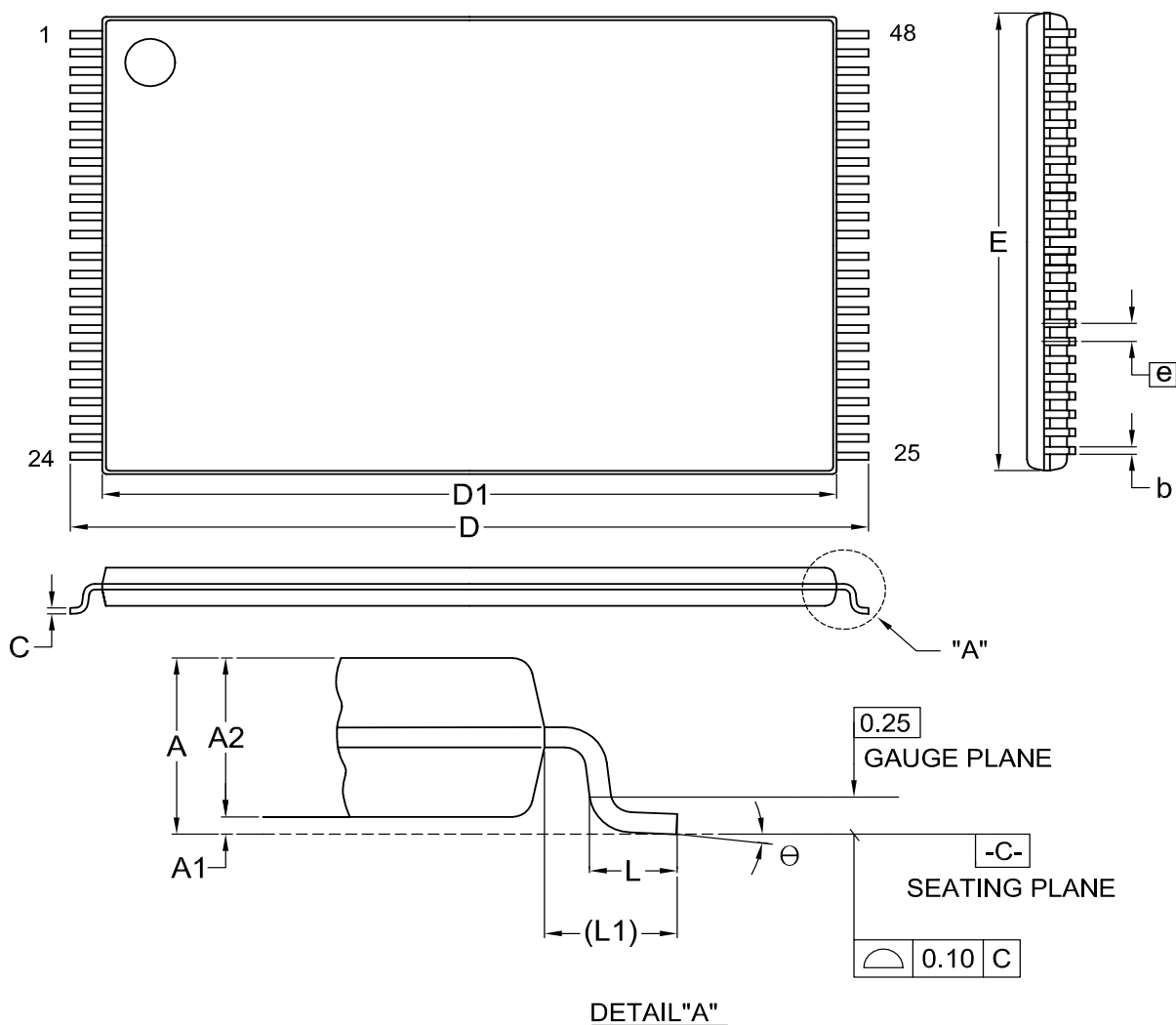
DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

	SYMBOL UNIT	A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	6	MO-142			09-24-'02

Title: **Package Outline for SOP 44L (500MIL)**

Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT	SYMBOL	A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	5	MO-175			09-24-'02

REVISION HISTORY

Revision No.	Description	Page	Date
1.1	Modified chip erase time to 13/35 sec	P16,37	MAY/09/2000
	Corrected content error	P11	
1.2	Add erase suspend ready max. 100us in ERASE SUSPEND's section at page10	P10	MAY/29/2000
1.3	Corrected content error at TOP BOOT SECTOR ADDRESS TABLE	P3	JUN/08/2000
1.4	To add the fast access time to 70ns	P1,14,16,38	DEC/04/2000
1.5	Modify Erase/Program Cycles:10,000 Cycles-->100,000 Cycles	P1,37	FEB/12/2001
1.6	To modify "Package Information"	P39~40	JUN/15/2001
1.7	To add I-grade (TA = -40°C TO 85°C)	P13~16,38	JUL/24/2001
1.8	1. Add automotive grade	P13~16,38	FEB/04/2002
1.9	1. To corrected typing error	All	JUN/06/2002
	2. To added bottom boot part no. in order information	P38	
2.0	1. Remove industrial grade	P14~16,38	AUG/13/2002
	2. Add remark of "under development" for automotive grade	P13~16,38	
	3. Standby current of automotive grade is 20uA max.	P14,38	
2.1	1. Re-define MX29F800T/B-70 test condition under output load: 1TTL gate + 30pF	P14,17	AUG/28/2002
2.2	1. Change tOES spec from 50ns to 35ns	P16	OCT/21/2002
	2. Modify package information	P39-40	
2.3	1. Added 48-TSOP with PB free package	P38	MAR/26/2003

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com